TMC1175AE1C

The Evaluation Board for the TMC1175AE1C

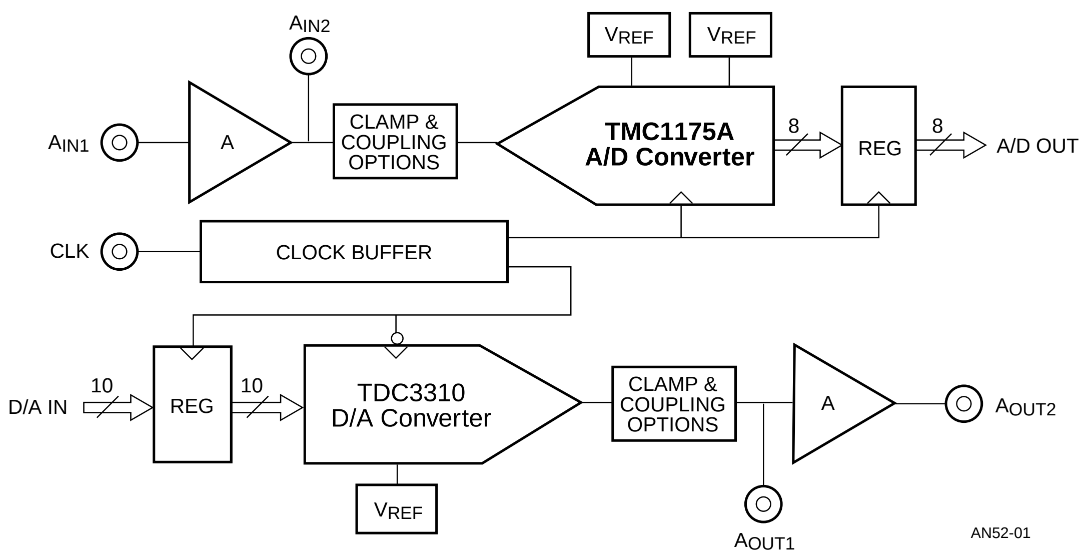
Description

The TMC1175AE1C Evaluation Board brings all of the circuitry together for evaluating Raytheon Electronics' TMC1175A CMOS A/D converter and the TDC3310 10-bit D/A converter. The A/D and D/A signal paths are independent but easily configurable at the edge connector for reconstruction of A/D converter data with the D/A converter. Data is registered after the A/D and before the D/A converters. A common clock signal will drive both A/D and D/A converters. A/D and D/A converters may also be clocked independently via the edge connector.

The TMC1175AE1C is a simple two-layer printed circuit board with 100 x 160 millimeter Eurocard dimensions. The component side of the board comprises mostly ground plane with only a few interconnections. A double row 64-pin DIN male connector gives access to all power and digital signals. Analog input and output signals are available from SMA connectors.

Variable voltage references are provided for the TMC1175A and TDC3310. Configurable input and output wideband video amplifiers are provided for signal conditioning. Signal path offsets may be adjusted at the input and output amplifiers.

Block Diagram



Power Supply and Clock Input Requirements

Both the TMC1175A and TDC3310 require only +5 Volts for operation. The A/D converter voltage reference circuits and wideband amplifiers may be operated from voltages of ±5 to ±18 Volts.

A Clock Buffer circuit has been included on the board with a 50Ω terminated SMA input. The clock buffer circuit provides separate CONV signals to the A/D and D/A converters and their registers. Pull-up resistors on edge-connector CLK inputs enable the clock buffer when a common clock is used. If separate clocks are desired, edge-connector pins B2 and B24 may be used for the A/D and D/A converters, respectively. The TDC3310 clock input may be monitored on test point TP1.

TMC1175A A/D Converter Circuitry

The circuitry included on this evaluation board is not intended to represent the minimum design for A/D operation. It is designed with maximum flexibility for evaluating the TMC1175A in various configurations.

The input amplifier, U6, may be configured for inverting or noninverting operation, with and without variable offset voltage. R39 is the potentiometer used for varying the offset of the signal applied to the A/D converter. The output of the input amplifier is monitored at SMA A_{IN2}. A_{IN2} may also be used as a signal input when AC-coupling to the A/D converter is used. The 75Ω input termination resistor and voltage gain of this amplifier are jumper selectable. Fixed amplifier gains of -4, -1, +2, and +5 are available.

AC- or DC-coupling directly to the TMC1175A is accomplished via input connector A_{IN2}. A “poor man’s” diode clamp limits the negative going AC-coupled signal to the A/D converter to the voltage applied to R_T. The diode clamp and coupling method are jumper selectable. Silicon diodes are included on the board to prevent voltage excursions on the input to the A/D converter from going beyond the power supply range.

Two variable voltage reference circuits are provided on the board for driving the R_T and R_B inputs of the TMC1175. The A/D reference voltage inputs may be jumper configured for the internal reference divider of the TMC1175A using V_{R+} and V_{R-}. Other jumper options connect R_T to V_{CC} and R_B to GND. The reference inputs to the A/D converter may be monitored on test points TP5 and TP6.

Table 1 summarizes the function of each jumper and Table 2 indicates which jumpers are to be installed and removed for amplifier configurations.

Table 1. A/D Converter Jumpers

J14	Connects OFFSET control to inverting input of amplifier.
J15	Grounds inverting input of amplifier for non-inverting operation.
J16	Connects A_{IN1} to inverting amplifier input.
J17	Enables 75Ω termination resistor on A_{IN1}
J18	Connects A_{IN1} to non-inverting amplifier input.
J19	Connects OFFSET control to non-inverting input of amplifier.
J20	Decreases feedback resistor of amplifier from 4.99kΩ to 1.0kΩ.
J21	Connects amplifier output to A/D input.
J22	DC couples amplifier output to A/D input.
J23	Enables 75Ω termination resistor on A_{IN2}.
J24	Enables diode clamp.
J25	Connects A/D R_T to V_{R+} pin.
J26	Connects A/D R_T to V_{CC}.
J27	Connects A/D R_T to variable voltage reference.
J28	Connects A/D R_B to ground.
J29	Connects A/D R_B to V_R pin.
J30	Connects A/D R_B to variable voltage reference.

Table 2. Jumpers for A/D Input Configurations

Configuration		Installed		Removed		
1	Non-inverting, with offset control	J14	J18	J15	J16	J19
2	Inverting, with offset control	J16	J19	J14	J15	J18
3	Non-inverting, without offset control	J15	J18	J14	J16	J19
4	AC-coupled direct input on A_{IN2} (with termination and clamp)	J23	J24	J21	J22	
5	DC-coupled direct input on A_{IN2} (without termination and clamp)	J22		J21	J23	J24

TDC3310 D/A Converter Circuitry

The D/A converter circuitry included on the Evaluation Board is not intended to represent the minimum design for D/A operation. It is designed with maximum flexibility for evaluating the TDC3310 in configurations that work for various applications and implementations. Since the TDC3310 is a 10-bit D/A converter, its two LSBs are jumpered to ground, enabling 8-bit operation, matching the resolution of the TMC1175A A/D converter. The INVERT input to the TDC3310 is grounded by jumper J4.

A simple band-gap voltage reference and potentiometer R7 provide a variable reference to the TDC3310. Varying R7 will change the “gain” of the TDC3310 D/A converter. The reference is set to -1.0 Volts with respect to the +5 Volt power supply as part of the factory test procedure. The adjustment ranges from -0.4 to -1.2 Volts with respect to the +5 Volt power supply. The TDC3310 reference voltage may be monitored on test point TP2.

AC- or DC-coupling directly from the TDC3310 to the output amplifier is accomplished via jumper J6. SMA connector A_{OUT1} can be used as a monitor point for the input to the output amplifier or as an un-amplified D/A converter output. A “poor man’s” diode clamp limits the negative going AC-coupled signal from the D/A converter to GND. The diode clamp is jumper selectable.

The wideband video output amplifier, U5, may be configured for inverting (A_V = -2) or noninverting (A_V = +2) operation with variable offset voltage from R16. The amplifier has an output series resistor of 75Ω to ensure 1 Volt pk-pk video levels into 75Ω terminated cables.

To reduce the common-mode power supply noise sensitivity of the output amplifier, the user can connect it differentially (Table 4, Configurations 5 through 8). Here, since the output of the D/A converter is referred to the +5 Volt power supply, the complementary input of the amplifier is resistively derived from the same supply. This configuration reduces the effect of common-mode noise from the power supply at the input to the amplifier.

Table 3 summarizes the function of each jumper and Table 4 indicates which jumpers are to be installed and removed for output amplifier configurations.

Table 3. D/A Converter Jumpers

J1	Enables 51Ω termination resistor on D/A CLK.
J2	Grounds LSB of D/A converter for 8-bit operation.
J3	Grounds 2nd LSB of D/A converter for 8-bit operation.
J4	Grounds INVERT input to D/A.
J5	Enables 75Ω termination resistor on A_{OUT1} connector.
J6	DC couples output of D/A converter.
J7	Enables diode clamp.
J8	Connects inverting input of amplifier to V_{CC}.
J9	Connects AC-coupled output of D/A to amplifier.
J10	Grounds inverting input of amplifier.
J11	Connects non-inverting input of amplifier to V_{CC}.
J12	Connects non-inverting input of amplifier to D/A output.
J13	Connects non-inverting input of amplifier to ground.

Table 4. Jumpers for D/A Output Amplifier Configurations

Configuration		Coupling	Referred	Installed			Removed				
1	Non-inverting	AC	GND	J10	J12		J6	J8	J9	J11	J13
2	Inverting	AC	GND	J9	J13		J6	J8	J10	J11	J12
3	Non-inverting	DC	GND	J6	J10	J12	J8	J9	J11	J13	
4	Inverting	DC	GND	J6	J9	J13	J8	J10	J11	J12	
5	Non-inverting	AC	V_{CC}	J8	J12		J6	J9	J10	J11	J13
6	Inverting	AC	V_{CC}	J9	J11		J6	J8	J10	J12	J13
7	Non-inverting	DC	V_{CC}	J6	J8	J12	J9	J10	J11	J13	
8	Inverting	DC	V_{CC}	J6	J9	J11	J8	J10	J12	J13	

The Edge Connector

The edge connector has been arranged to easily configure the board for reconstructing A/D data with the TDC3310 D/A converter. A/D data outputs are located exactly adjacent to D/A data inputs on the edge connector. Simply shorting these edge connector pins together will enable the direct transfer of data from one signal path to the other.

Table 5. Edge-connector Pin Assignments

A32	GND	B32	V– (-15V)
A31	GND	B31	V+ (+15V)
A30	GND	B30	N/C
A29	GND	B29	N/C
A28	GND	B28	N/C
A27	GND	B27	N/C
A26	GND	B26	N/C
A25	GND	B25	N/C
A24	GND	B24	D/A CONV Input
A23	GND	B23	N/C
A22	GND	B22	N/C
A21	D/A D_1 MSB	B21	A/D D_1 MSB
A20	D/A D_2	B20	A/D D_2
A19	D/A D_3	B19	A/D D_3
A18	GND	B18	V_{CC} (+5V)
A17	D/A D_4	B17	A/D D_4
A16	D/A D_5	B16	A/D D_5
A15	D/A D_6	B15	A/D D_6
A14	D/A D_7	B14	A/D D_7
A13	D/A D_8	B13	A/D D_8 LSB
A12	D/A D_9	B12	N/C
A11	D/A D_{10} LSB	B11	N/C
A10	N/C	B10	N/C
A9	N/C	B9	N/C
A8	N/C	B8	N/C
A7	N/C	B7	N/C
A6	N/C	B6	N/C
A5	N/C	B5	N/C
A4	GND	B4	N/C
A3	GND	B3	N/C
A2	GND	B2	A/D CONV Input
A1	GND	B1	V_{EE} (-5.2V)

Schematic Diagrams

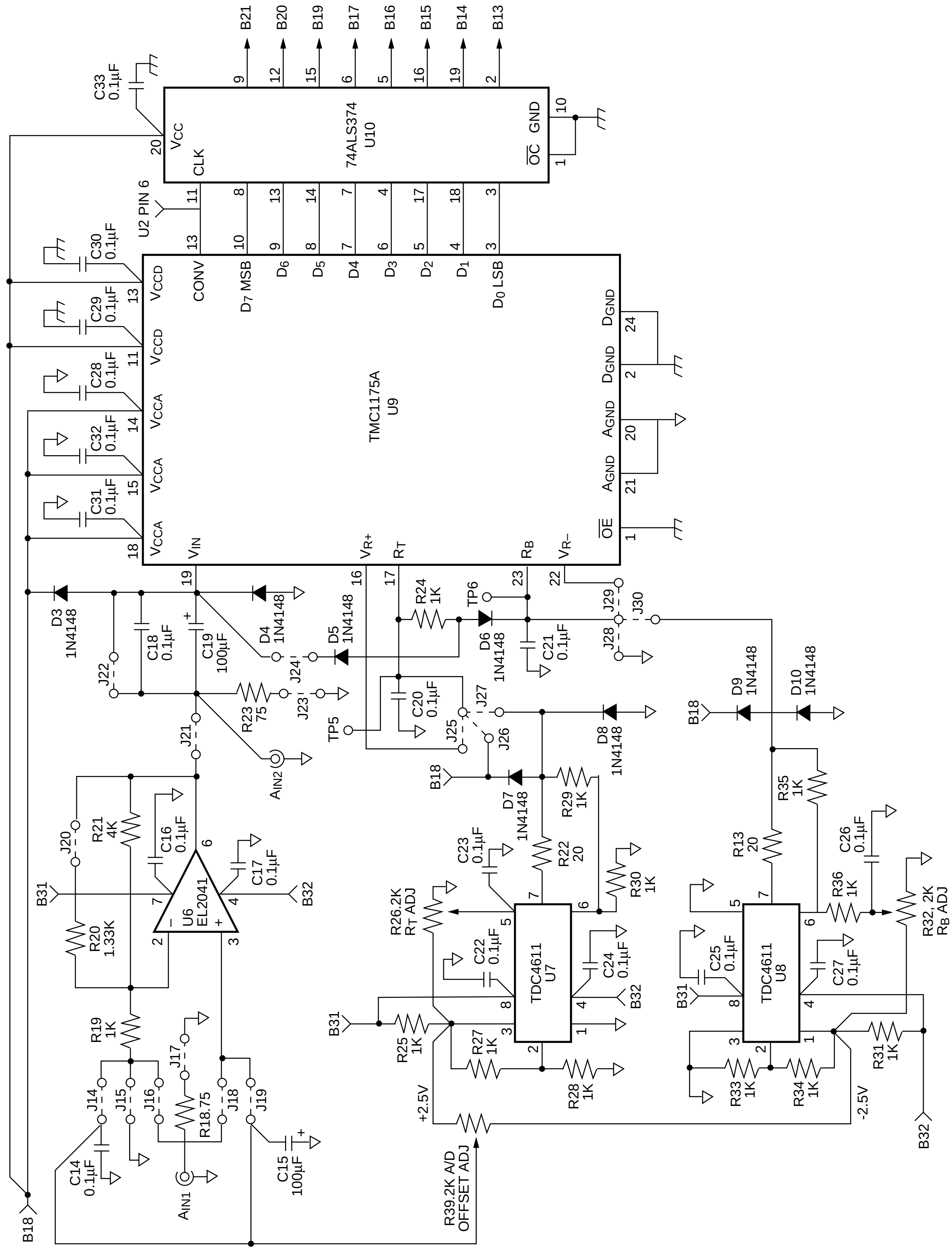


Figure 2. A/D Converter

Schematic Diagrams (continued)

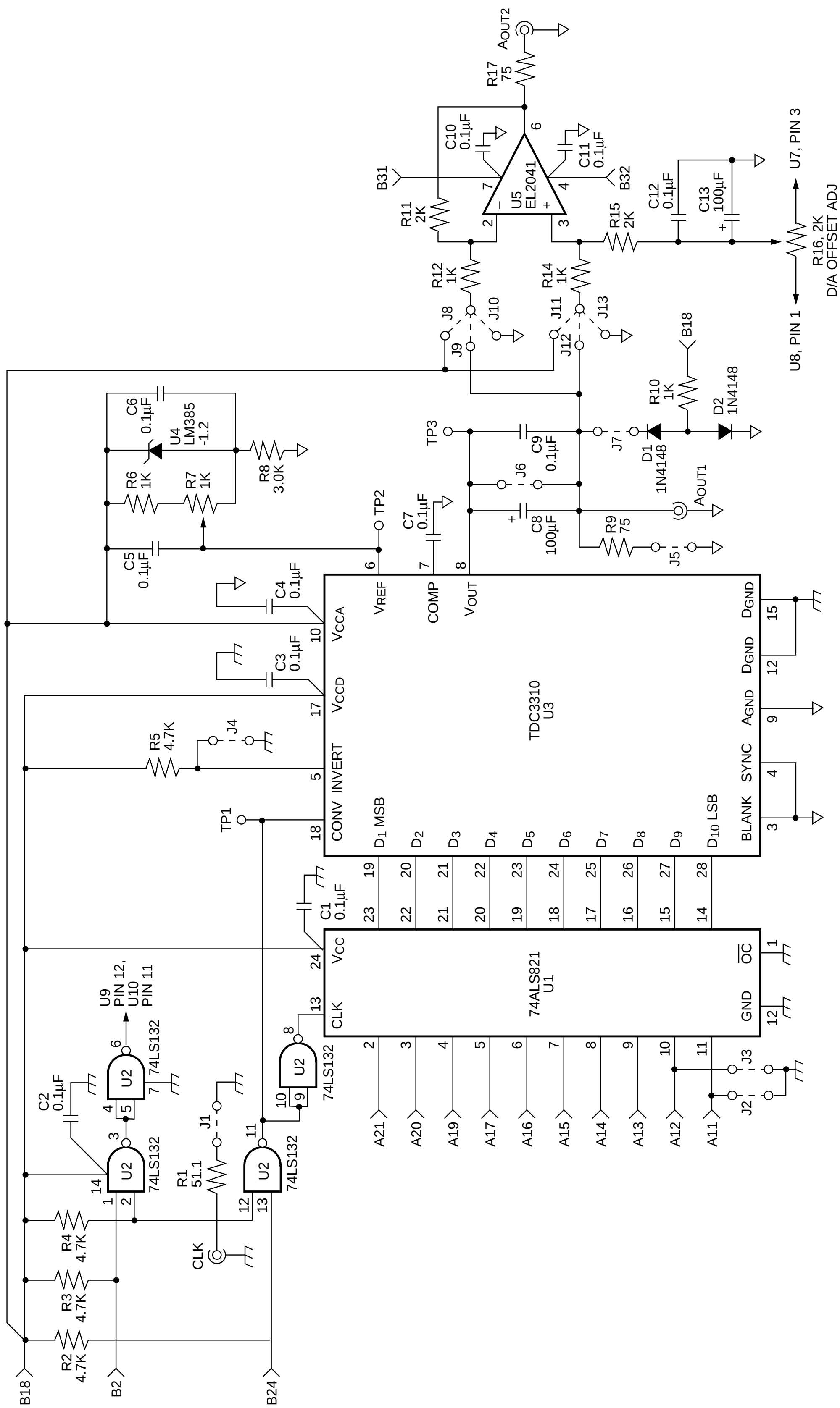


Figure 3. D/A Converter

Table 6. Parts List

Item	Qty	Part/Value	Ref. Designator	Mfg. P/N
1	1	Resistor, 51.1Ω	R1	RN55D51R1F
2	4	Resistor, 4.75kΩ	R2-R5	RN55D4751F
3	16	Resistor, 1.0kΩ	R6, R10, R12, R14, R19, R24-R25, R27-R31, R33-R36	RN55D1001F
4	1	Potentiometer, 2kΩ	R7	RJ26FW202
5	1	Resistor, 2.94kΩ	R8	RN55D2941F
6	4	Resistor, 75Ω	R9, R17, R18, R23	RN55D75R0F
7	2	Resistor, 2.0kΩ	R11, R15	RN55D2001F
8	2	Resistor, 20Ω	R13, R22	RN55D20R0F
9	4	Potentiometer, 2kΩ	R16, R26, R32, R39	3006Y-1-202, 3006P-1-202
10	1	Resistor, 1.30kΩ	R20	RN55D1301F
11	1	Resistor, 4.02kΩ	R21	RN55D4021F
12	29	Capacitor, 0.1µF, 50WVDC, 20% Tol.	C1-C7, C9-C12, C14, C16-C18, C20-C33	AVX: SR215E104MAA, CK05BX104K Kemet: C322C104M5U5CA, C052C104K5X5CA Murata-Erie: RPE122Z5U104M50V
13	4	Capacitor, 100µF, 10WVDC, 20% Tol.	C8, C13, C15, C19	AVX: TAP107K010HSB Kemet: T354E107K01AS
14	1	10-bit register	U1	74AS821NT
15	1	Quad NAND	U2	74LS132N
16	1	10-bit Video D/A	U3	TDC3310N6C, Raytheon
17	1	Reference 1.2 V	U4	LT1004CH-1.2
18	2	Video Amplifier	U5, U6	EL2041CN
19	2	Reference/Amplifier	U7, U8	LM611CN, National
20	1	8-bit A/D	U9	TMC1175AN2C, Raytheon
21	1	8-bit Register	U10	74ALS374
22	10	0.2 AMP 100V D035	D1-D10	1N4148
23	1	Eurocard Connector DIN 41612 2-Row 64-Contact Board Mount Male		Amphenol 704-C133-714A-64P, Winchester 64P-6033-0430
24	5	SMA Coax Connector	AIN1, AOUT2, CLK, AIN2, AOUT1	Omni-Spectra 2062-0000-00, Sealectro 50-561-000-31
25	1	24 Pin DIP 0.300" Row Spacing I.C. Socket	U9	Robinson-Nugent ICA-243-S-TG or Equivalent
26	1	28 Pin DIP 0.600" Row Spacing I.C. Socket	U3	Robinson-Nugent ICA-286-S-TG or Equivalent
27	7	0.025" Square Post Header, 2 Contacts 0.100" Spacing	J1, J4-J7, J20, J23	Robinson-Nugent NSH-02SB-S2-TR
28	1	0.025" Square Post Header, 3 Contacts 0.100" Spacing	J18-J19	Robinson-Nugent NSH-03SB-S2-TR
29	1	0.025" Square Post Header, 4 Contacts 0.100" Spacing	J2-J3	Robinson-Nugent NSH-04DB-S2-TR
30	1	0.025" Square Post Header, 6 Contacts 0.100" Spacing	J21-J22, J24	Robinson-Nugent NSH-06DB-S2-TR

Table 6. Parts List (continued)

Item	Qty	Part/Value	Ref. Designator	Mfg. P/N
31	1	0.025" Square Post Header, 8 Contacts 0.100" Spacing	J14-J17	Robinson-Nugent NSH-08DB-S2-TR
32	2	0.025" Square Post Header, 12 Contacts 0.100" Spacing	J8-J13, J25-J30	Robinson-Nugent NSH-12DB-S2-TR
33	11	Header Programming Shunts	J6, J9, J11, J14, J17, J18, J20-J22, J27, J30	Robinson-Nugent HPS-03-G
34	1	Universal Transistor Mount	U4	Bivar 111-80
35	2	2-56 x 7/16 Machine Screws		
36	2	2-56 Nuts		
37	2	#2 Flat Washer		
38	2	#2 Locking Washer		
39	1	Bare P.C. Board TMC1175/ TDC3310E1C Rev. B		

PC Board Layout

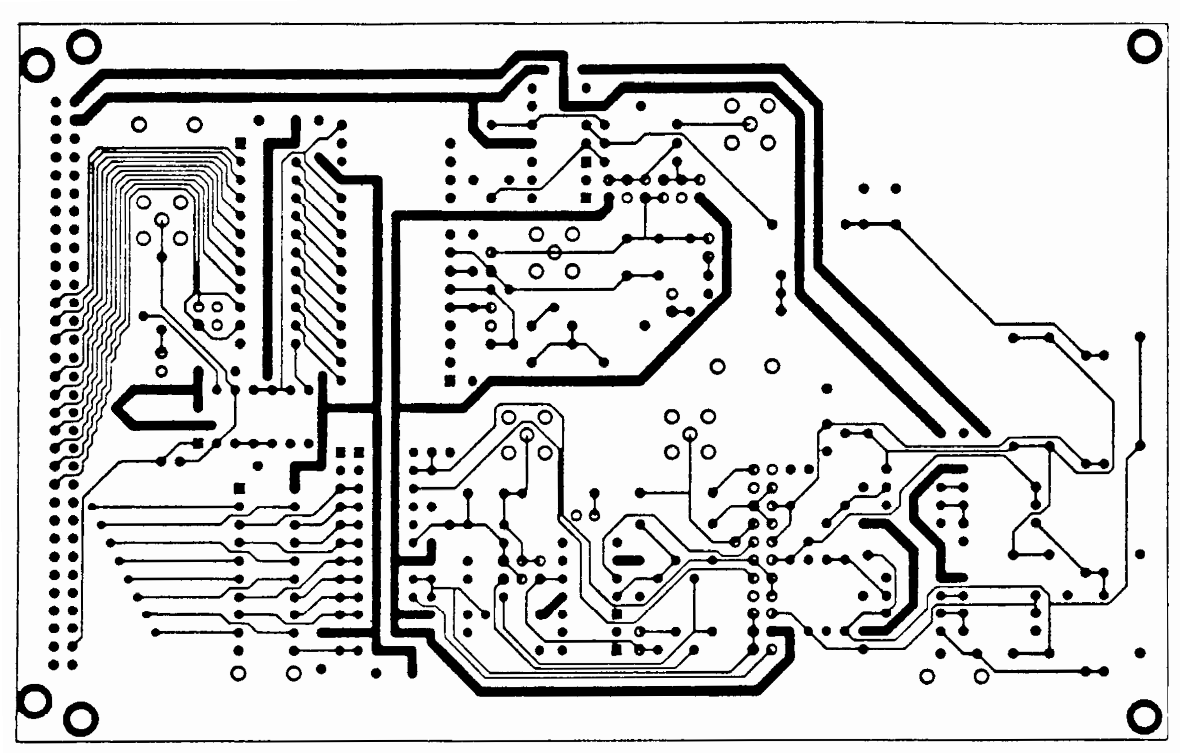


Figure 4. PC Board Circuit-Side Layout

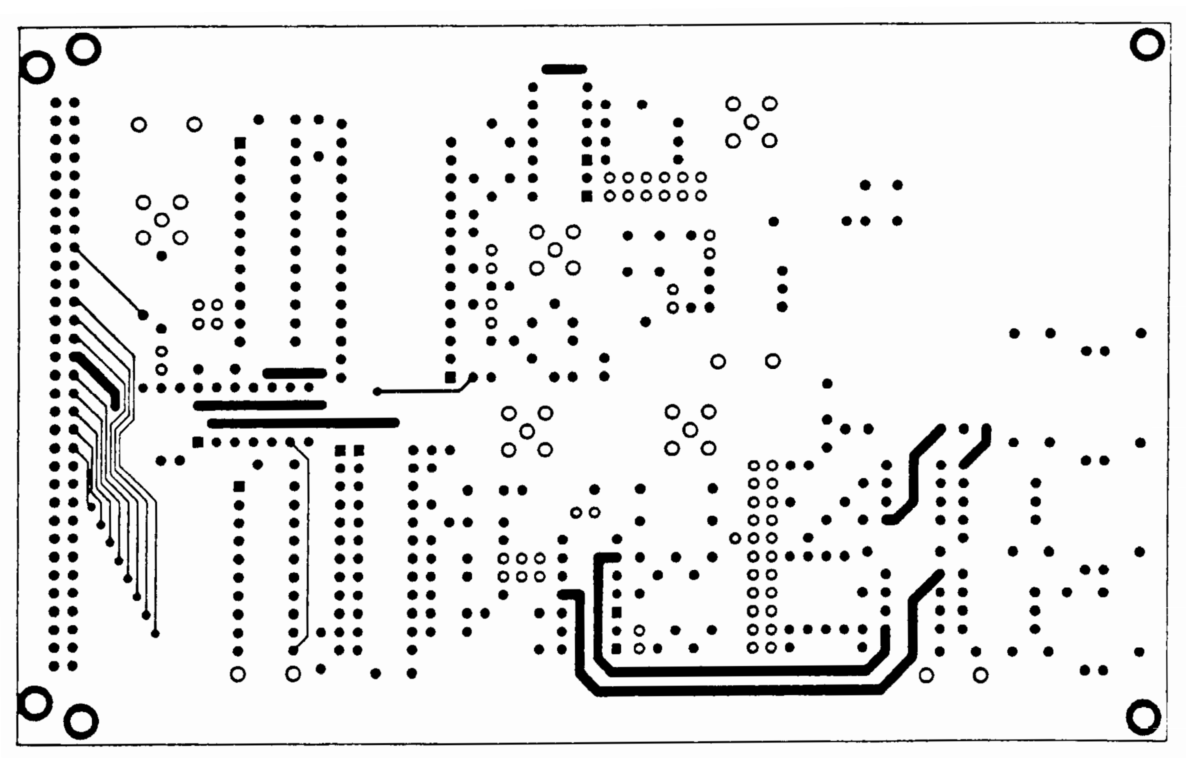


Figure 5. PC Board Component-Side Layout

PC Board Layout (continued)

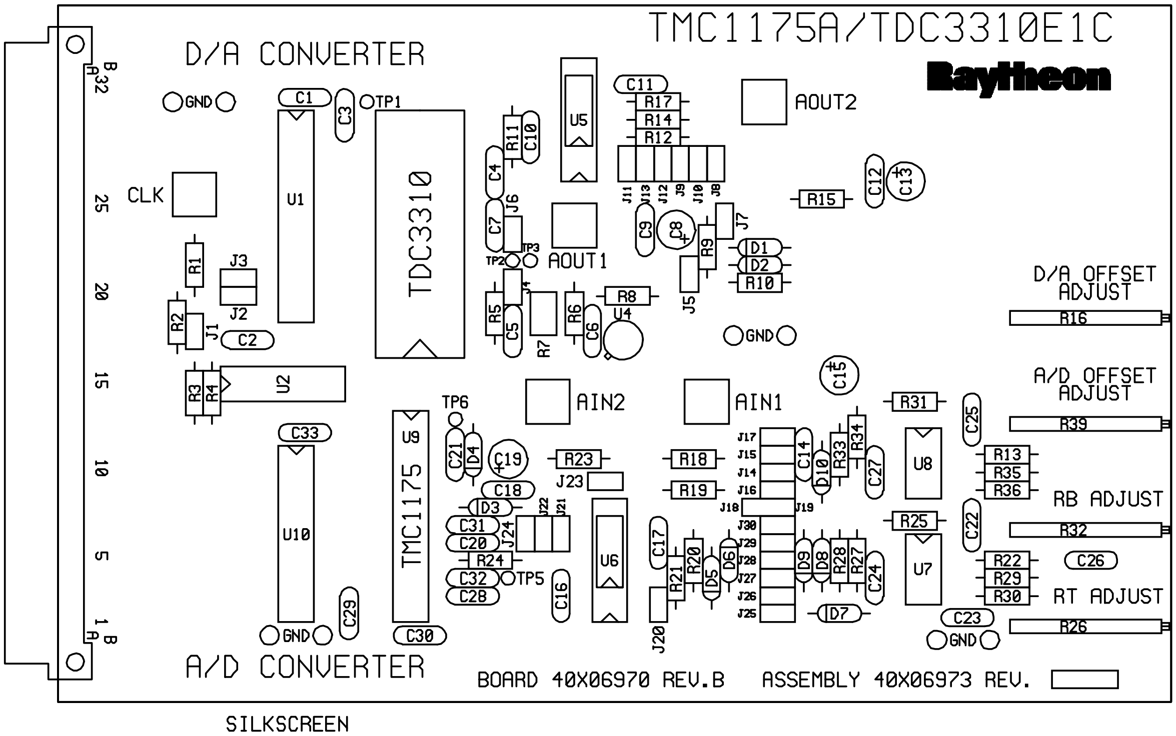


Figure 6. PC Board Silkscreen Layout

Notes:

LIFE SUPPORT POLICY:

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